

1/10

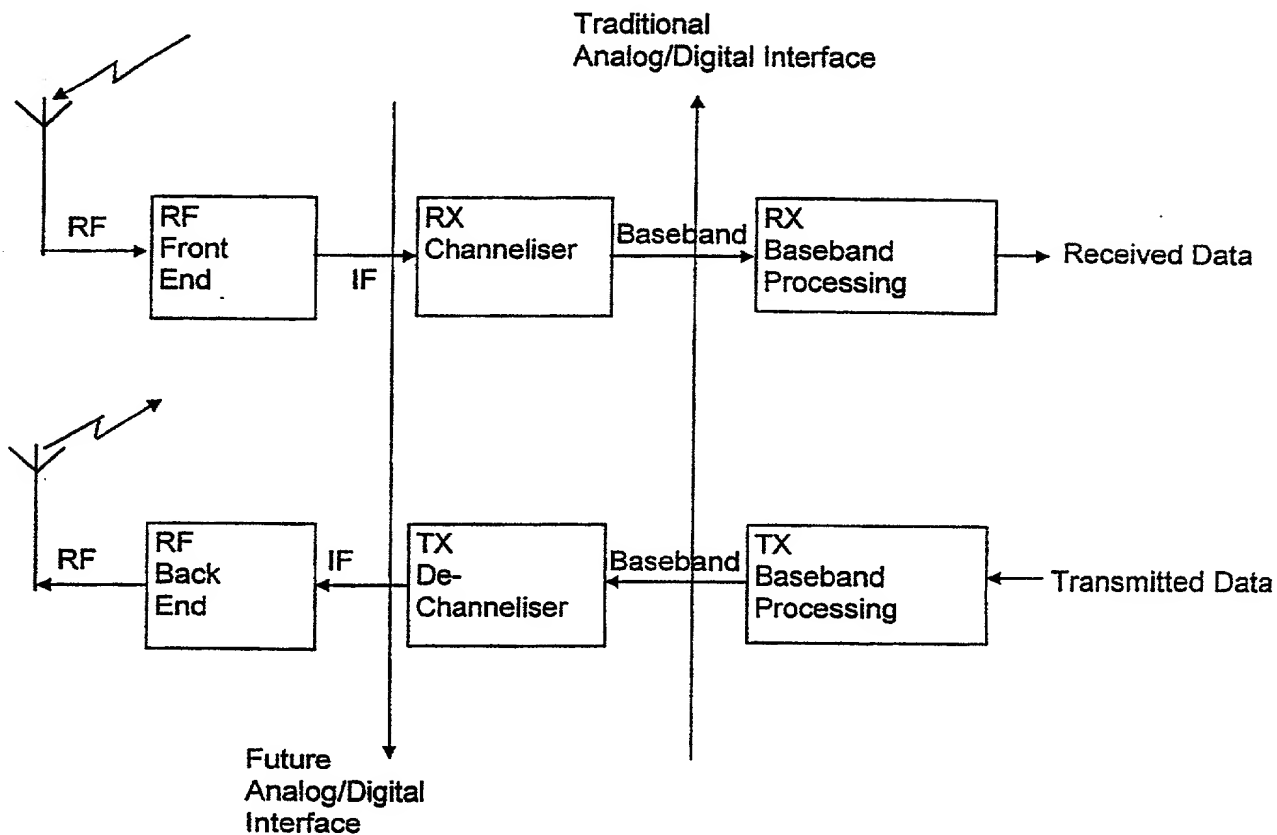
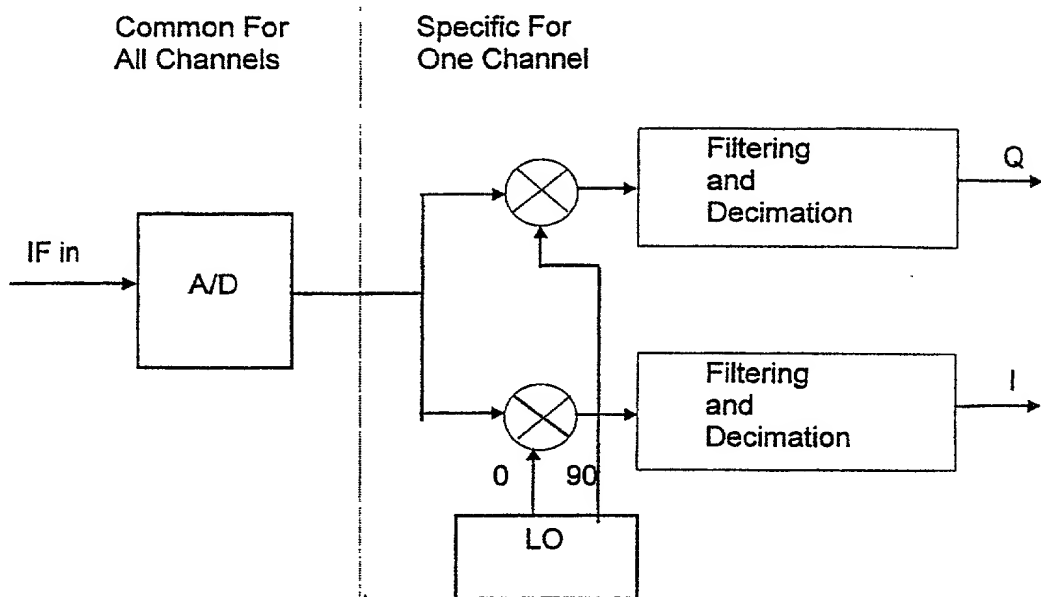


Fig. 1

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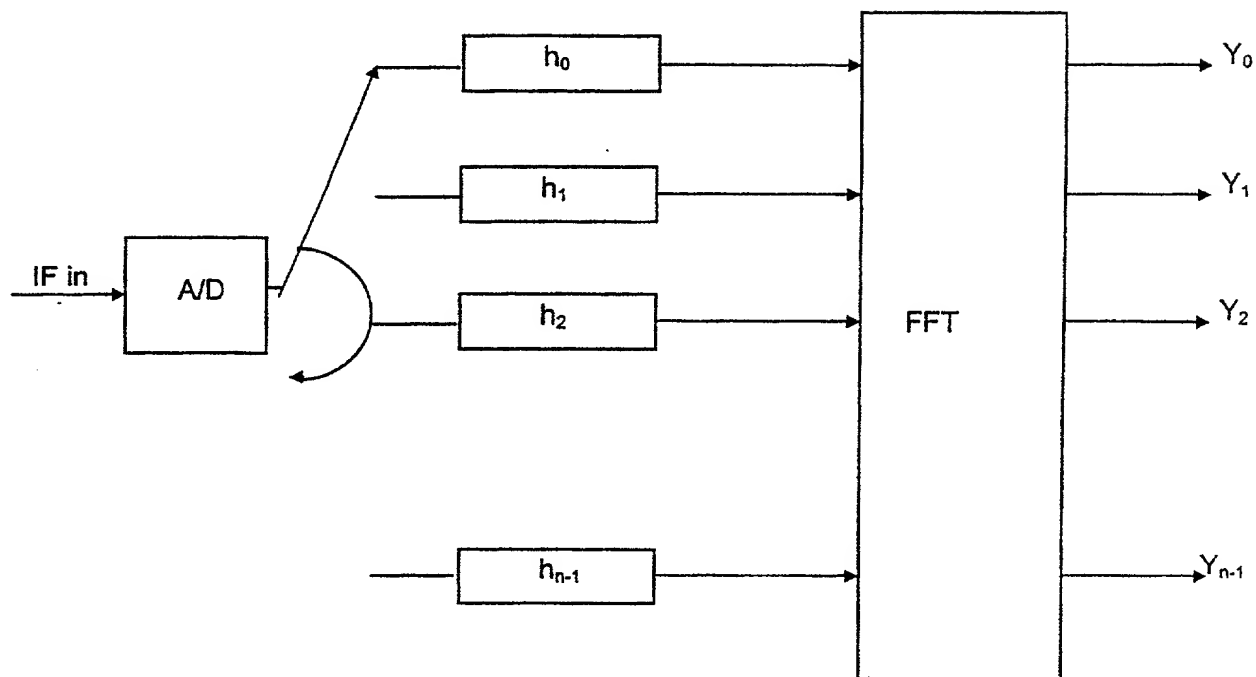


Receiver Channeliser Implemented as an
IQ Channeliser

Fig 2

003250-235-120200

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Receiver Channeliser Implemented Via
A Decimated Filter Bank

Fig. 3

003250-235 120800



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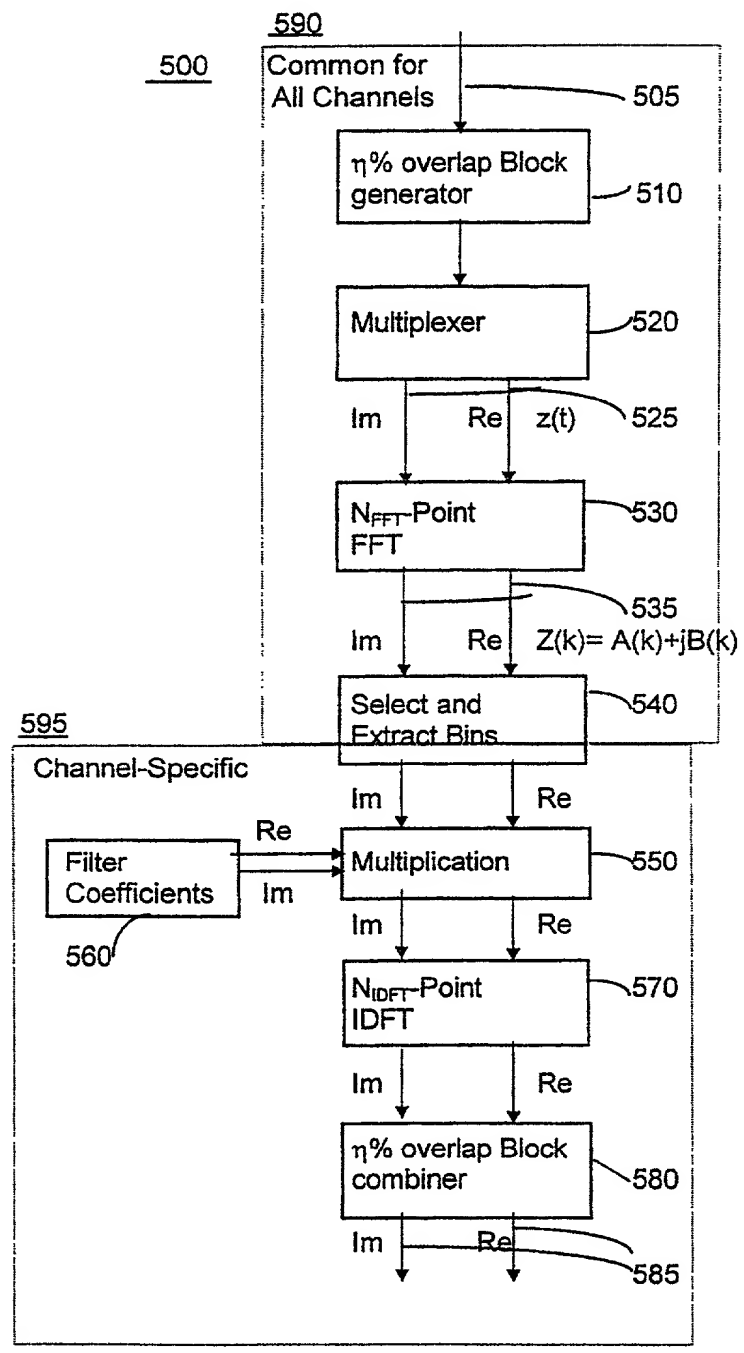


Fig. 5

0034775-100000

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600

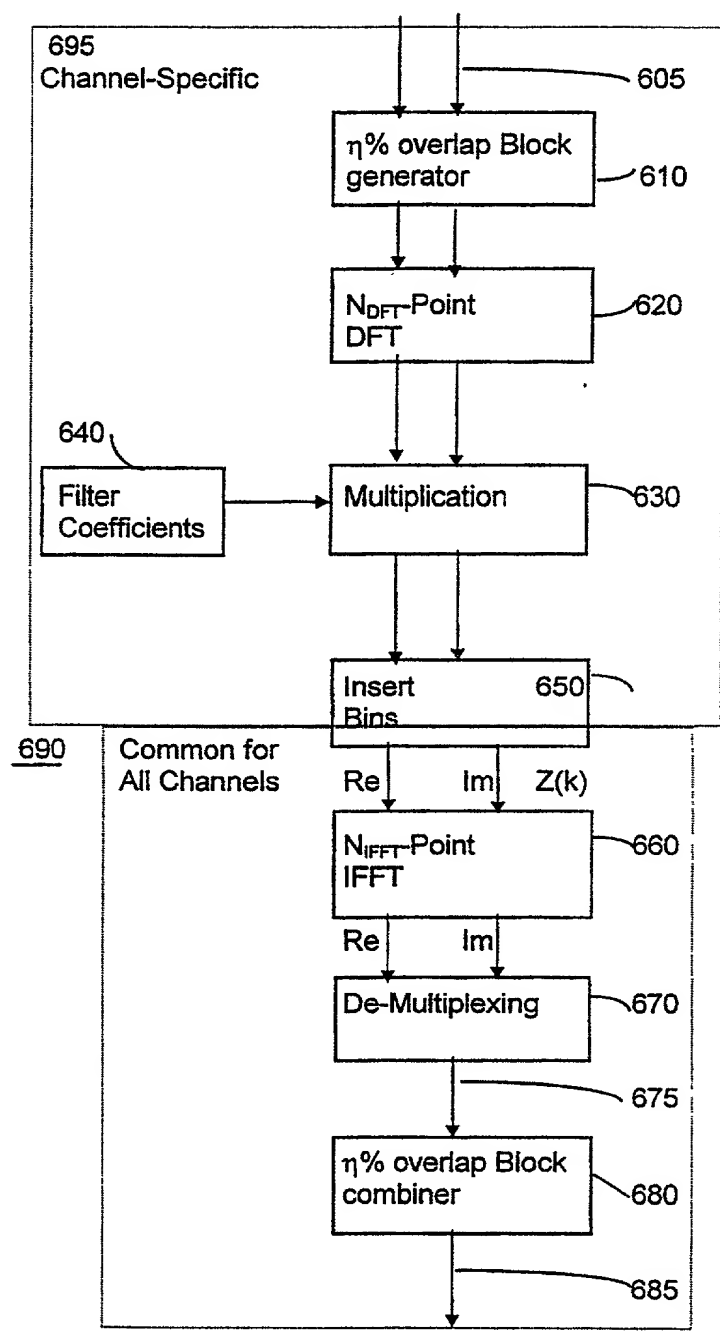
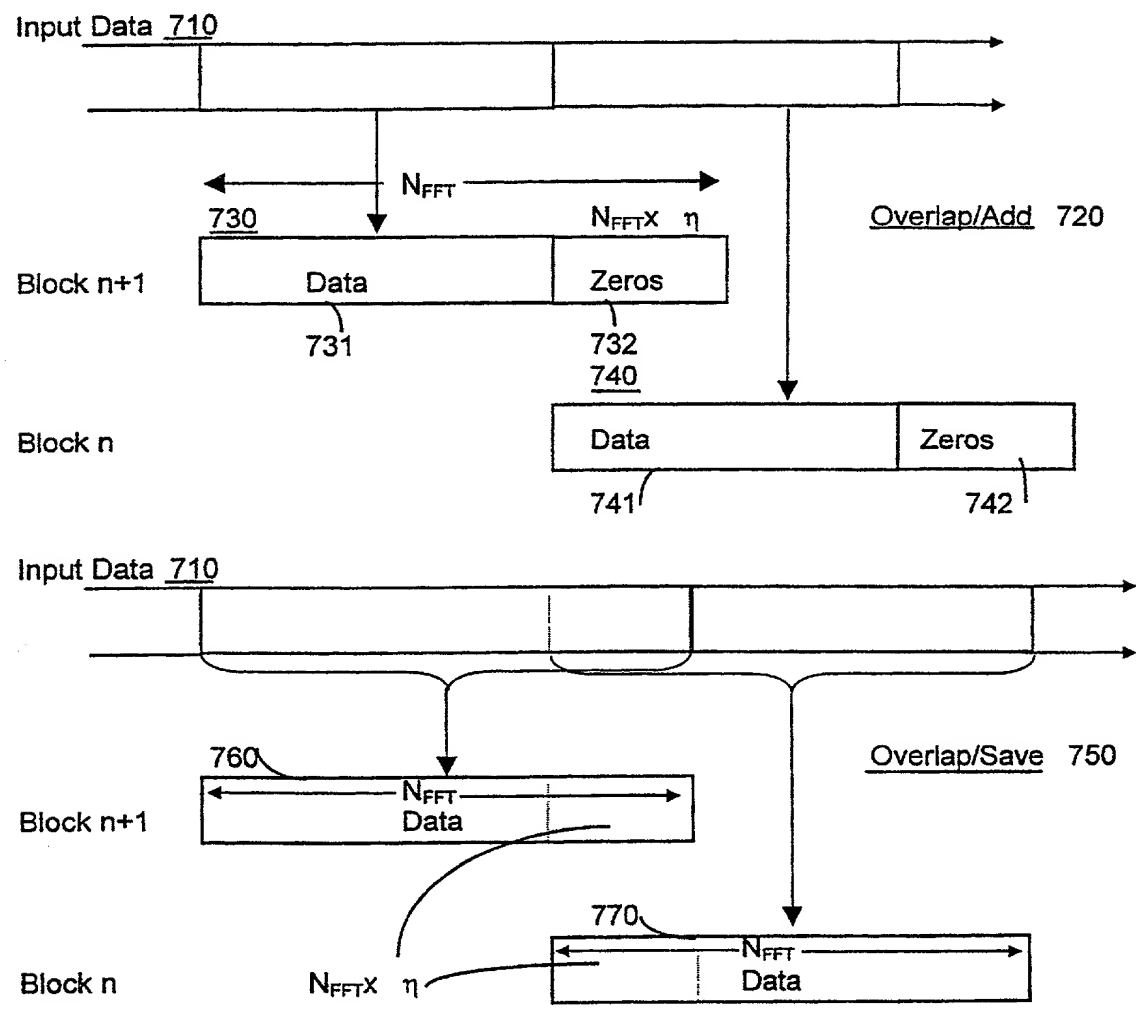


Fig. 6

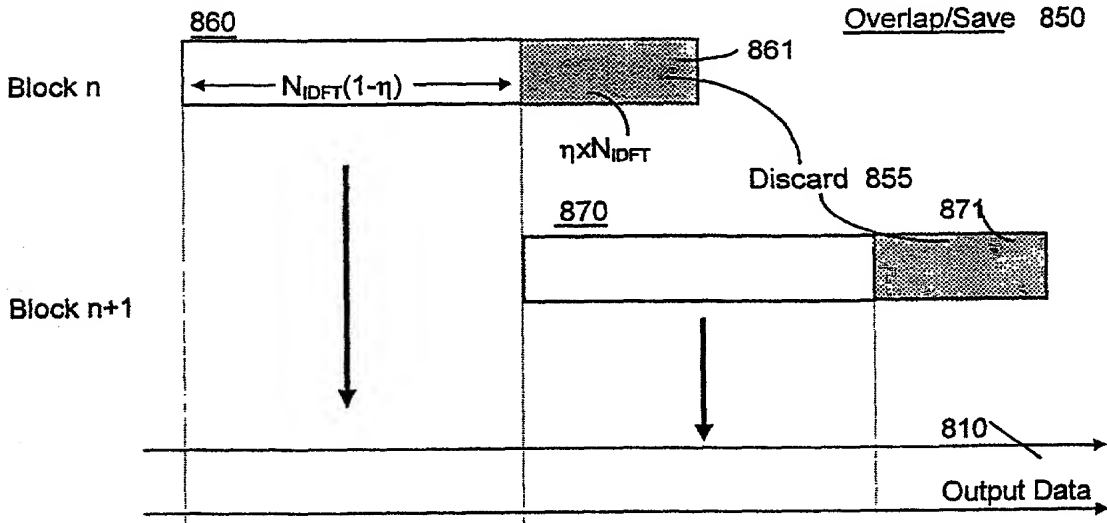
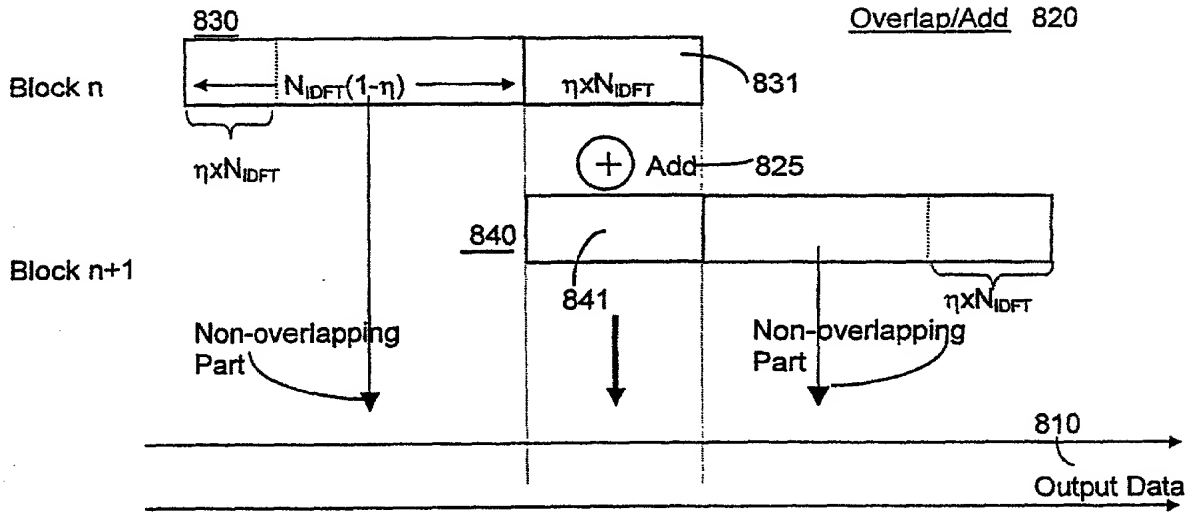
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$\eta\%$ Overlap Block Generator

Fig. 7

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$\eta\%$ Overlap Block Combiner

Fig. 8

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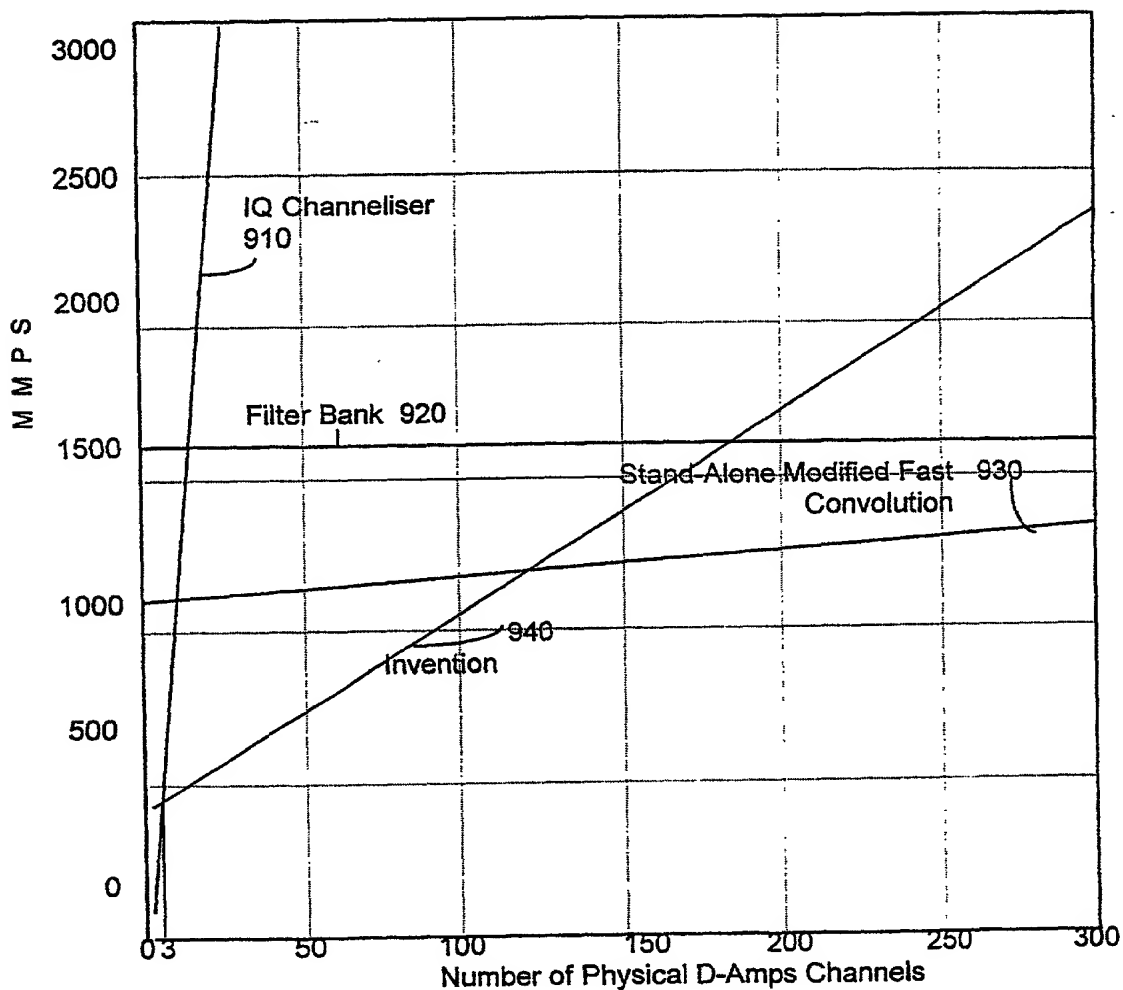


Fig. 9

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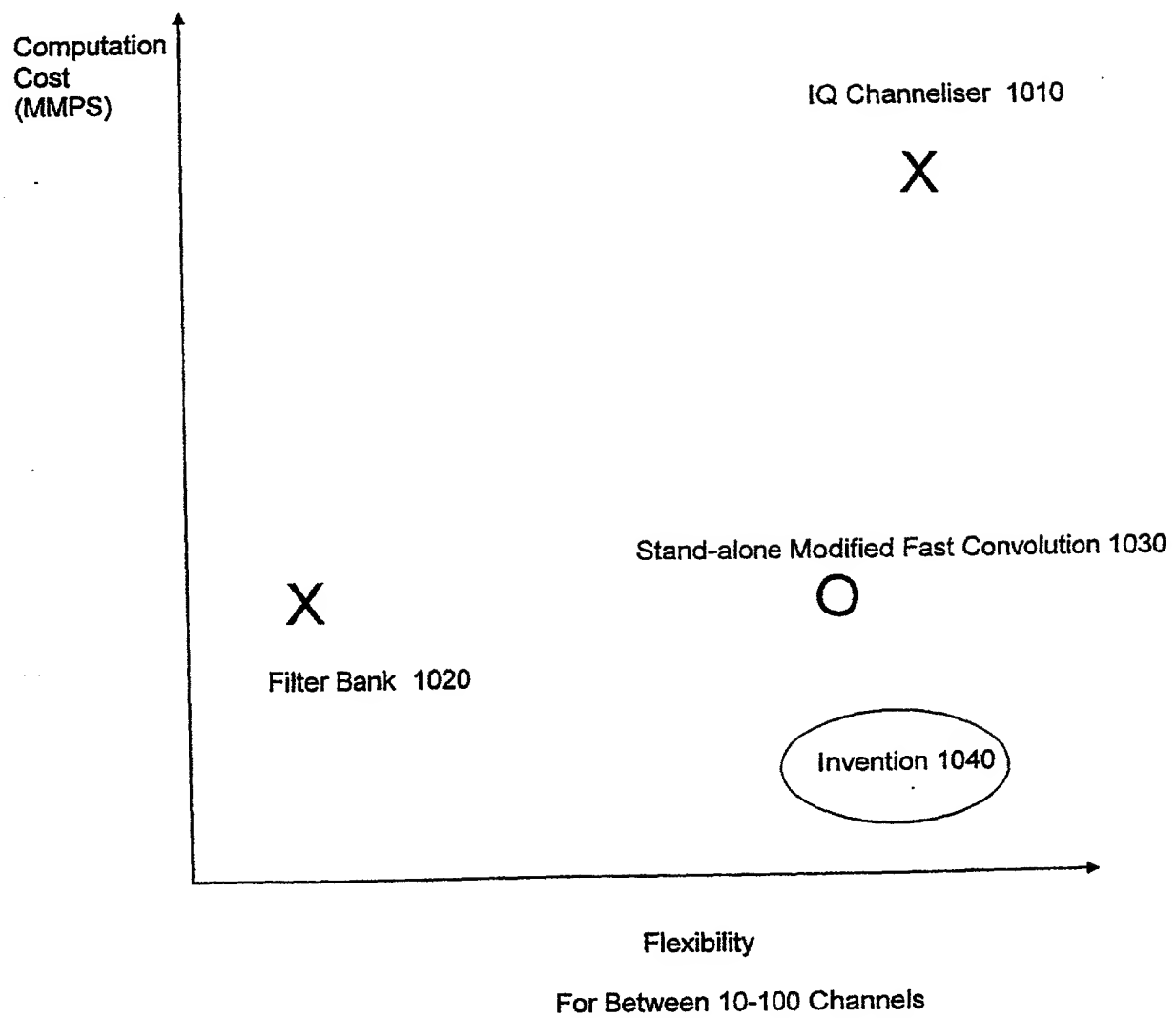


Fig. 10